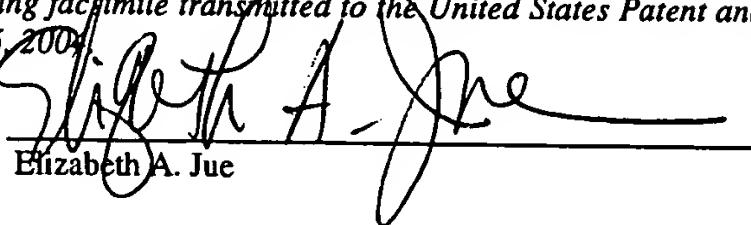


DATE OF NOTICE
OF ALLOWANCE: March 18, 2004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office at (703) 872-9306 on April 5, 2004.


Elizabeth A. Jue

Appl No. : 09/383,150 Confirmation No. 6176
Applicant : Rong-Fuh Shyu
Filed : August 25, 1999
Title : LEAD FRAME FOR A SEMICONDUCTOR CHIP PACKAGE,
SEMICONDUCTOR CHIP PACKAGE INCORPORATING MULTIPLE
INTEGRATED CIRCUIT CHIPS, AND METHOD OF FABRICATING A
SEMICONDUCTOR CHIP PACKAGE WITH MULTIPLE INTEGRATED
CIRCUIT CHIPS

TC/A.U. : 2826
Examiner : Fetsum Abraham

Docket No. : 35761/DBP/S295

Customer No. : 23363

AMENDMENT UNDER 37 CFR § 1.312

Office of Initial Processing
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Post Office Box 7068
Pasadena, CA 91109-7068
April 5, 2004

Commissioner:

Prior to the payment of the issue fees, Applicant would like the following amendments entered.

IN THE CLAIMS

Claims 1-8. (Previously cancelled).

Please cancel originally filed claims 9-13.

Please renumber incorrectly numbered claims 9-12 added in the Amendment filed on June 23, 2003, as follows:

14. [9.] (Currently amended) A semiconductor chip package, comprising:

a lead frame including a frame body, at least two chip-receiving windows formed in said frame body, a plurality of internal connection leads formed on said frame body adjacent to said chip-receiving windows, and a plurality of external connection leads formed on said frame body adjacent to at least one of said chip-receiving windows; and

at least two integrated circuit chips, each of which is received in a respective one of said chip-receiving windows and has a plurality of bonding pads formed thereon, wherein said internal connection leads are electrically connected to said bonding pads on said at least two integrated circuit chips in said at least two chip-receiving windows to establish internal electrical connection among said at least two integrated circuit chips, wherein one of said integrated circuit chips is a master integrated circuit chip, and another of said integrated circuit chips is a slave integrated circuit chip, wherein said master integrated circuit chip includes an embedded testing circuit to permit testing of said slave integrated circuit chip that is connected thereto during a testing process of said semiconductor chip package.

15. [10.] (Currently amended) The semiconductor chip package as claimed in Claim [9] 14, wherein said internal connection leads are wire-bonded to said bonding pads on said at least two

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integrated circuit chips in said at least two chip-receiving windows.

16. [11.] (Currently amended) The semiconductor chip package as claimed in Claim [9]14, wherein there are no external connection leads to any bonding pads on said slave integrated circuit chip, said external connection leads serving as terminal pins such that external electrical connection with said slave integrated circuit chip is established only via said master integrated circuit chip.

17.12. (Currently amended) The semiconductor chip package of Claim [9]14, wherein for the testing process of said semiconductor chip package, said master integrated circuit chip is configured to receive stimulating signals via said external connection leads to stimulate said at least one slave integrated circuit chip via said internal connection leads in response to the stimulating signals, to receive stimulation response of said at least one slave integrated circuit chip via said internal connection leads, and to output information corresponding to the stimulation response via said external connection leads.

REMARKS/ARGUMENTS

Applicant has received a notice of allowance in this case, having a due date of June 18, 2004.

In the review of the case file, Applicant noticed a numbering error with the allowed claims, and request correction of the claim numbering.

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The initial application was filed with claims 1-13. On November 30, 2000, the Examiner issued a restriction requirement stating that two groups of claims were present in the application, namely, Group I, with claims 1-8, drawn to a package of a device, and Group II, with claims 9-13, drawn to a method of making a packaging device.

On December 26, 2000, Applicant elected Group I, directed to claims 1-8, drawn to a packaging device, but did not cancel claims 9-13.

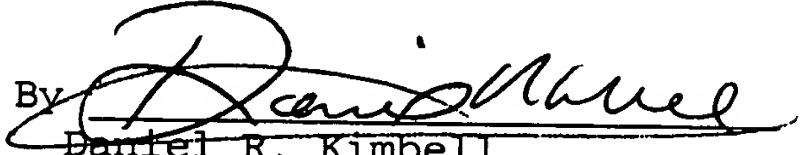
The elected claims 1-8 were rejected, and on February 3, 2003, Applicant canceled claims 1-8, and added new claims 9-12. However, new claims 9-12 should have been numbered as claims 14-17 rather than as claims 9-12. This error was noticed by neither the Examiner nor by the Applicant at the time. Thereafter, the new, misnumbered claims 9-12 were rejected by the Examiner. On June 23, 2003, Applicant amended misnumbered claims 9-12. This amendment resulted in the allowance of misnumbered claims 9-12.

In order to rectify this error and correct the record, Applicant requests that originally filed claims 9-13 be canceled and that misnumbered claims 9-12 (that have been allowed) be renumbered as claims 14-17 and thereafter be issued as claims 1-4.

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If the Examiner and or the Issue Branch have any questions,
a telephone call to the undersigned would be appreciated.

Respectfully submitted,
CHRISTIE, PARKER & HALE, LLP

By 
Daniel R. Kimbell

Reg. No. 34,849
626/795-9900

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